REMARKS

This Amendment seeks to place this application in condition for allowance. All of the Examiner's rejections have been addressed. Several of the pending claims have been amended to more particularly point out the claimed subject matter. Several dependent claims have been added. No new matter has been added.

OFFICE ACTION

In the Office Action mailed March 13, 2002 (hereinafter, "the OFFICE ACTION"), claim 151, and the claims that depend therefrom, were found to be allowable. Independent claims 164 and 173 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent No. 4,823,321 to Aoyama (hereinafter, "Aoyama"). Finally, the claims which depend from independent claims 164 and 173 were objected to as being dependent upon a rejected base claim, but were found to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. These rejections are addressed below.

35 USC 102(b) Rejection

In the OFFICE ACTION, independent claims 164 and 173 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 4,823,321 to Aoyama (hereinafter, "Aoyama"). It is respectfully submitted that independent claims 164 and 173 present patentable

subject matter. Applicants address the rejection to each of the independent claim separately below.

Claim 164 is not anticipated under 35 USC 102(b)

Applicants submit that claim 164 (in its previous or amended form) is not anticipated by Aoyama. Claim 164 is directed to a method of controlling a synchronous memory device and recites in part "issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value...."

Applicants submit that Aoyama does not disclose, for example, a method of controlling a memory device that includes issuing an operation code which initiates an access of a programmable register in the memory device. Aoyama, to the extent understood, describes a FIFO memory which includes a register situated in the data-path between the memory cell array and data output buffer[1]. That register is merely used to temporarily store data read from the memory cell array, before that data is output by the buffer (e.g., "...the data read from the memory cell array 1 is temporarily stored in the register 12 and is output as the output data D_{out}", col. 3, lines 35-37, '321 patent). Moreover, the register disclosed in Aoyama is not programmable as claimed in the instant application, but merely serves as temporary storage for data to be

[1] For example, register 12, data output buffer 10 and memory cell array 1 in Fig. 4 of Aoyama.

provided to the output buffer after that data is accessed from the memory cell array.

Thus, for at least those reasons, claim 164 is not anticipated by Aoyama.

Notwithstanding the foregoing, Applicants have amended claim 164 to more particularly point out and distinctly claim the invention. In this regard, Applicants have amended claim 164 to include, in part, "issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value, wherein the binary value is representative of control information ...."

Claim 173 is not anticipated under 35 USC 102(b)

For similar reasons given above with respect to claim 164, Applicants submit that claim 173 (in it's previous or amended form) is also not anticipated by Aoyama. In this regard, the register disclosed in Aoyama is not programmable as is claimed in claim 173. Instead, the register of Aoyama serves to temporarily store data before the data is provided to the output buffer.

Thus, for at least that reason, claim 173 is not anticipated by Aoyama.

Notwithstanding the foregoing, however, Applicants have amended claim 173 to more particularly point out and distinctly claim the invention. In this regard, Applicants have amended claim

162 to recite in part "a programmable register to store a binary value that is representative of control information".

Prior Art Made of Record

Applicants acknowledge the prior art made of record but not relied upon, namely U.S. Patent 4,445,204 (hereinafter, "the '204 patent"). It is not clear what is meant by the Examiner's characterization of the '204 patent (i.e., "a memory device having a circuit for selectively deriving a count signal from one of the count of output terminal to a programmed state"). However, in order to present a more concise response to the OFFICE ACTION, and because the Examiner tacitly acknowledges that the '204 patent does not impact the patentability of any of the claimed inventions, Applicants will not comment on that characterization. No inference or conclusion should be drawn that Applicants agree, in any way, with the Examiner's characterization of the '204 patent. Indeed, no inference or conclusion of any kind should be drawn from the absence of Applicants' comment pertaining to that characterization.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks and amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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Jose G. Moniz
Reg No. 50,192

Rambus Inc.
4440 El Camino Real
Los Altos, CA 94022
650-947-5336

Exhibit A -- Version with Markings to Show Changes Made

164. (Amended) A method of controlling a synchronous memory device by a controller, wherein the memory device includes an array of memory cells and a programmable register, the method of controlling the memory device comprises:

issuing a first operation code to the memory device, wherein the first operation code initiates an access of the programmable register in the memory device in order to store a binary value, wherein the binary value is representative of control information; and

providing the binary value to the memory device, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

165. (Amended) The method of claim 164 wherein the [binary value] control information is representative of a number of clock cycles of an external clock signal to transpire before the memory device outputs data in response to a second operation code.

173. (Twice Amended) A synchronous memory device including an array of memory cells, the synchronous memory device comprises:

clock receiver circuitry to receive an external clock signal;

input receiver circuitry to sample a first operation code synchronously with respect to a transition of the external clock signal; and

a programmable register to store a binary value that is representative of control information, wherein the memory device stores the binary value in the programmable register in response to the first operation code.

174. (Amended) The memory device of claim 173 wherein the [binary value] control information is representative of a number of clock cycles of the external clock signal to transpire before the memory device outputs data and wherein the memory device outputs data in response to a second operation code.

183. (Amended) The method of claim 164 wherein the first operation code is issued to the memory device via an external bus.